CLAIMS

What is claimed is:

1. A data optimization engine for deoptimizing selected frames of a first stream of data, comprising:

a receive interface circuit coupled to an optimization processor, said receive interface circuit being configured for receiving said first stream of data, said receive interface circuit includes

a traffic controller circuit for separating frames in said first stream of data into a first deoptimizable frame and a first non-deoptimizable frame, and

a deoptimization front-end circuit coupled to said traffic controller circuit to receive at least a first portion of said first deoptimizable frame, said deoptimization front-end circuit including a protocol conversion circuit configured to convert data in said first portion of said first deoptimizable frame from a first protocol to a second protocol suitable for processing by said optimization processor, said first protocol specifies a first word length, said second protocol specifies a second word length different from said first word length,

wherein said optimization processor is configured to deoptimize said first portion of said first deoptimizable frame by performing at least one of decompression and decryption on said first portion of said first deoptimizable frame.

2. The data optimization engine of claim 1 wherein said first protocol is the 10-bit interface protocol, and said protocol conversion circuit includes a 10-bit/8-bit lookup table.

3. The data optimization engine of claim 2 further including a frame alignment circuit having an output coupled to said traffic controller circuit, said frame alignment circuit being configured for detecting and aligning a start of a primitive signal word in said first stream of data with a start of a reference 40-bit word, thereby framing said primitive signal word with respect to said reference 40-bit word.

4. The data optimization engine of claim 3 wherein said frame alignment circuit detects said start of said primitive signal word by monitoring for a K28.5 10-bit word in said first stream of data.

5. The data optimization engine of claim 1 further including an output FIFO coupled to said traffic controller circuit and said deoptimization front-end circuit, said traffic controller circuit further includes a start-of-frame handler circuit and an end-of-frame handler circuit, said start-of-frame handler circuit is configured detect a start-of-frame 40-bit word in said first deoptimizable frame and to send said start-of-frame 40-bit word to said output FIFO, effectively bypassing said deoptimization front-end circuit, said end-of-frame handler circuit is configured to detect an end-of-frame 40-bit word in said first deoptimizable frame and to temporarily retain said end-of-frame 40-bit word while waiting for said deoptimization processor to complete deoptimizing said first portion of said first deoptimizable frame, said end-of-frame handler circuit is further configured to furnish a polarity-correct version of said end-of-frame 40-bit word to said output FIFO for appending to first deoptimized data within said output FIFO, said first deoptimized data represents a first deoptimized version of said first portion of said first deoptimizable frame after being deoptimized by said optimization processor.

6. The data optimization engine of claim 5 wherein said receive interface circuit further includes an end-of-deoptimized-data flag handler circuit coupled to receive second deoptimized data from said optimization processor, said second deoptimized data represents a second deoptimized version of said first portion of said first deoptimizable frame after being deoptimized by said optimization processor, said end-

of-deoptimized data flag handler being configured to detect an end-of-deoptimized data flag in said second deoptimized data and signals, upon detecting said end-of-deoptimized data flag in said second deoptimized data, said end-of-frame handler circuit to furnish said polarity-correct version of said end-of-frame 40-bit word to said output FIFO.